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Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials

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Standard Test Structures For Reliability Assessment of AlCu Metallizations with Barrier Materials

(From JEDEC Board Ballot JCB-00-105, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. The barrier material might exist in one or all of the following locations:

- Above and/or below the aluminum-copper metal layer, and
- Above and/or below the contact or via to connect metal layers.
- Barrier materials commonly include, but would not be limited to: tungsten (W), titanium (Ti), titanium-nitride (TiN), titanium-aluminide (Ti_2Al_3), and platinum (Pt).

This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems.

Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers.

Throughout this document, the term “via” is used to describe design of a conductive path between conductive metal layers. This term is also used to describe a conductive path between doped Si or poly-Si and a metal conductor that might also be referred to as a “contact”.

The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

2 Test structure design issues

2.1 Kelvin connection

All structures must allow Kelvin connections for resistance measurement. Each end of the metal resistor lines must have 1) a connection to source/sink high currents, and 2) a connection for voltage monitor.

2.2 Line width

At line widths greater than the median grain size, electromigration proceeds via grain boundary diffusion. Lines with multiple grains across the line width must be evaluated for reliability.

The narrowest line width allowed by layout design rules must be assessed. As line width gets narrower than median grain size, commonly referred to as bamboo grains, electromigration will not be dominated by grain boundary diffusion and reliability of the line will be different than for wider lines.

2.3 Line length

2.3.1 Short lines

When a line is short, back diffusion of metal ions can slow or stop electromigration [*]). To ensure that electromigration is being properly assessed, the test line must be sufficiently long to ensure that no or minimal back diffusion of ions will slow void growth.

2.3.2 Long lines and failure criterion

With barrier material interconnect systems, after copper depletion in the AlCu line, electromigration structures on most processes (but not all processes) will gradually increase in resistance until the pre-defined resistance-increase failure criterion has been reached. The resistance increase is caused by EM voiding and is a direct measure of the EM rate. Failure criterion is usually a fractional increase in the starting resistance; such that the starting resistance (or starting line length) defines, to a large extent, when the failure criterion might be meet. Provision must be made to standardize, or otherwise normalize, line-length effects on time-to-failure.

* I. Blech, “Electromigration in Thin Aluminum films on Titanium Nitride”, J. Appl. Phys., 47, 1976, pp. 1203.

2 Test structure design issues (cont'd)

2.4 Reservoirs

It has been shown †), ‡), §) that areas and/or volumes of metal surrounding vias, often referred to as “reservoirs”, can have significant impact on electromigration in barrier material interconnect systems; however, a complete understanding of these effects is not presently available. Given the significant impact that reservoirs have, test structure design must be very specific in the regions surrounding the vias to be used with a given failure and acceptance criterion.

2.5 Extrusion monitor

Monitoring for metal extrusions is important. Placement of monitor lines at minimum spacing from the stress lines allows for appropriate extrusion monitor and provides a level of optical loading that will tend to produce test lines with final dimensions closer to those likely to be found in a typical design. Use of additional lines for optical loading is not restricted by this standard. Placement of a single, isolated, minimum dimension lines may yield unrepresentative line widths and should be avoided.

3 Electromigration test structure definition: Line and Via structures

3.1 Structure introduction

For each "new" metal-layer/Via combination, build structures to assess reliability of a particular metal-line/barrier combination using the characteristics (see also Figure 1):

- Kelvin connected, wide source lines,
- extrusion monitors,
- narrow lines with single via (to upper and/or lower barrier),
- wide lines with vias (to upper and/or lower barrier), and
- all needed combinations of via-to-line.

† M. Dion, “Electromigration Lifetime Enhancement for Lines with Multiple Branches ” Proceedings of the 38th International Reliability Physics Symposium, 2000, pp. 324.

‡ E. Atokav, "Effect of VLSI Interconnect Layout on Electromigration Performance," Proceedings of the 36th International Reliability Physics Symposium, 1998, pp. 348.

§ B. Baerg, "Recent Problems in Electromigration," Proceedings of the 35th International Reliability Physics Symposium, 1997, pp. 211.

3 Electromigration test structure definition: Line and Via structures (cont'd)

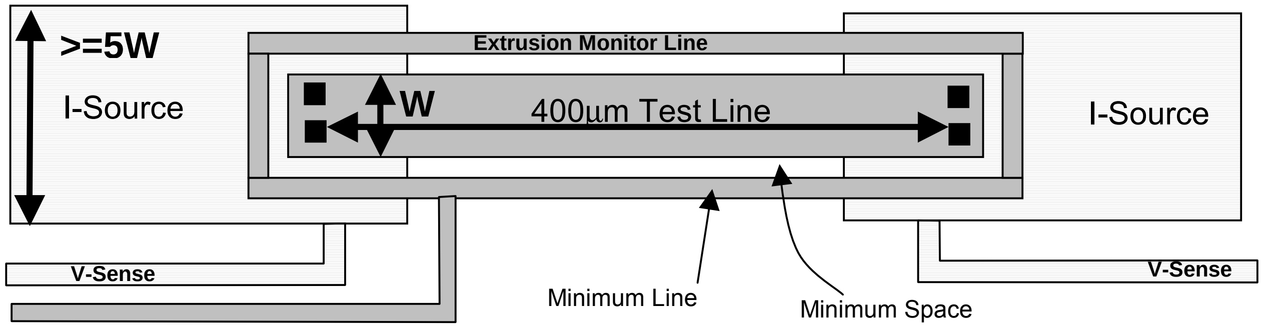

Figure 1—An example barrier metal EM structure, with Kelvin connected wide current source lines, extrusion monitor lines, a non-minimum width 400 µm long test line connected through vias. Many other configurations are possible.

3.2 Very wide source line

Very wide current source lines are at both ends of the structure and should be greater than or equal to 5 times the test line width.

3.3 Voltage sense (to allow Kelvin connection)

Voltage sense lines will be connected to the wide current feed lines at each end of the structure, adjacent and as close as possible to the vias to the test line. The voltage sense lines will not be directly connected to the test line since they could act as reservoirs.

3.4 Extrusion monitor

Along the length and on each side of the test line there will be lines on both sides to sense for shorting by metal extrusions or whiskers. The extrusion lines will be of minimum allowed width and separated from the test line by the minimum allowed space.

3.5 Narrow line, with single via

- In designing a narrow line structure, the following dimensions are important: minimum line width, minimum via size, minimum overlap of metal to via, and minimum space between lines. Design of the narrow line with a single via can have different configurations depending upon the relative values.
- Use single contact/via and minimum width line:
- 1 Contact or Via at the cathode end of a line.
- Minimum line width
- Minimum metal overlap over/around/below the Via
- Test line length =400 µm (length>>Blech length, constant length for ΔR failure criterion). See also 3.7.

3 Electromigration test structure definition: Line and Via Structures (cont'd)

3.6 Wide lines

1) Wide lines can fail for electromigration differently than narrow lines. It is important to stress lines that have multiple metal grains across the line width. Other characteristics are similar to those of the narrow, single via line.

2) Length =400 µm (>>Blech length). See also 3.7.

3) If the median AlCu grain size is known, then line width shall be ≥ 3 times the grain size, otherwise line width shall be ≥ 3 µm. However, getting vias to fit in the line width, with minimum spaces and overlaps will often dictate the line width. Select the wide-line width and number of vias connected to the line such that:

   a) At the cathode end(s), vias must span the width of the line, with minimum spaces and overlaps, and

   b) line width is either greater than or equal to 3 X (median grain size)

   –OR-

   c) line width is greater than or equal to 3 µm.

4) The line will have a single row of vias across the line width, at the end of the line for the metal-barrier interface. Minimum via-to-via spacing and minimum metal overlaps of via must be used. Available test equipment must be capable of stressing the line widths used.

5) It is recommended that maximum joule heating [**]) at the maximum stress current be less than 10 °C.

[**] JEDEC Standard 33A (JESD33A), "Standard Method for Measuring and using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line."

3 Electromigration test structure definition: Line and Via Structures (cont'd)

3.7 Line length alternatives

When a 400 µm test line is not available, it is "possible" to normalize measured data from an arbitrary length line to that of a 400 µm test line. Following the procedure published by Ann Witrouw, et al. [††]), experimentation and modeling are used to obtain EM failure characteristic model parameters for a structure of a given length (initial resistance - Ro, incubation time – t_i, maximum resistance change possible – ΔRmax, a time constant - τ, and constant - p_c). Given these parameters is possible to model an equivalent lifetime for a 400 µm, standard structure length, with all other design features being the same. Attempts using this alternative should be documented with procedure and intermediate results.

3.8 Connection to current tap

Three (3) current tap to test-line designs types would be acceptable (others may be equally acceptable) .

3.8.1 Mirror design

Top or bottom metal feed to lower metal as seen in Figure 2. This design can be used to source electron current from either end, and can be flipped vertically to evaluate another metal-via combination.

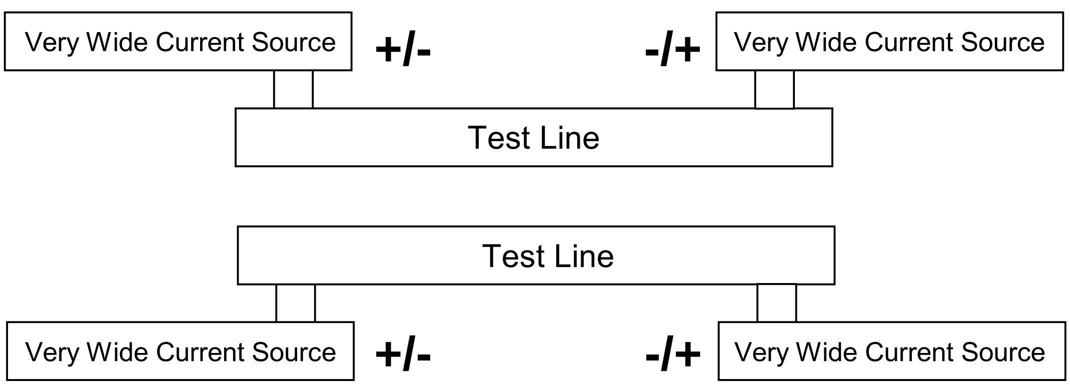

Figure 2 — A structure with mirror images at either end increases the flexibility at assembly and test. It is easily flipped for stressing of other levels.

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†† A. Witrouw, "Incubation, Time-Dependent Drift and Saturation During Al-Si-Cu Electromigration: Modeling and Implications for Design," Proceedings IITC, 1998, pp. 27.

3.8 Connection to current tap (cont'd)

3.8.2 Top and bottom feed to metal line

The barrier interface evaluated depends upon the source of the electron current (cathode). In the figure, if the electron current comes from the top metal (left), then the upper via to the test line is properly evaluated. If the electron current comes from the bottom metal (right), then the lower via to the test line is properly evaluated. See Figure 3.

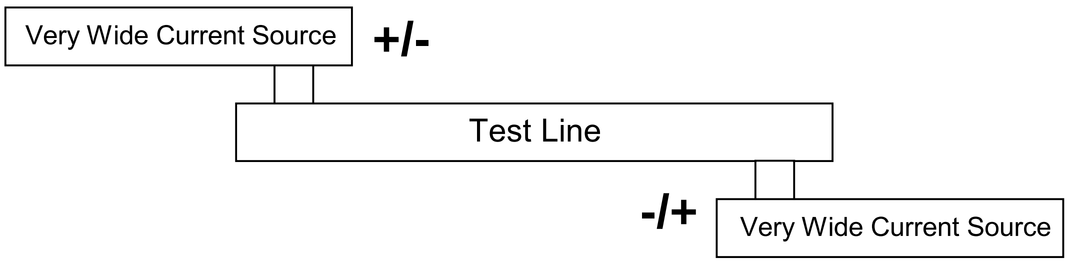

Figure 3 — A structure with top and bottom current feed at opposite ends allows two via-to-line interfaces to be tested; however, careful experiment planning and execution are needed to ensure the correct current direction is applied.

3.8.3 Single via ended

The single ended structure can be used to stress a via-to-line interface or just the metal line; care must be taken when interpreting barrier material interconnect system EM data when vias are not used. See Figure 4.

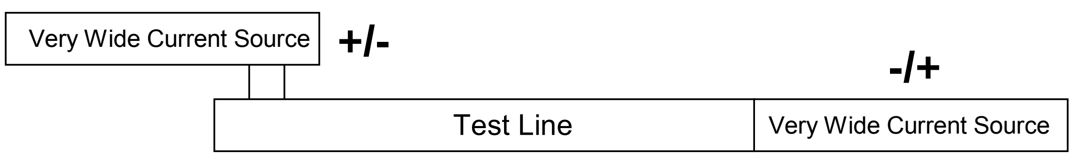

Figure 4 — Single via ended EM structure.

3 Electromigration test structure definition: Line and Via Structures (cont'd)

3.9 Via-to-Line configuration: Reservoir development

As discussed in section 2.4 the size and location of metal surrounding the vias has a significant impact on EM results. Therefore the metal dimensions used in the region surrounding the via must represent design layout ground rule minimum dimensions. Depending upon the minimum line width and the size of the via, the via plus minimum overlaps may or may not fit within the minimum allowed line width, as shown in Figure 5.

If layout design rules allow extra metal or "reservoir additions" to surround the via (increasing reservoir size beyond design rule minimums) and also allow higher currents with those additions, structures must be available that demonstrate the larger allowed reservoirs.

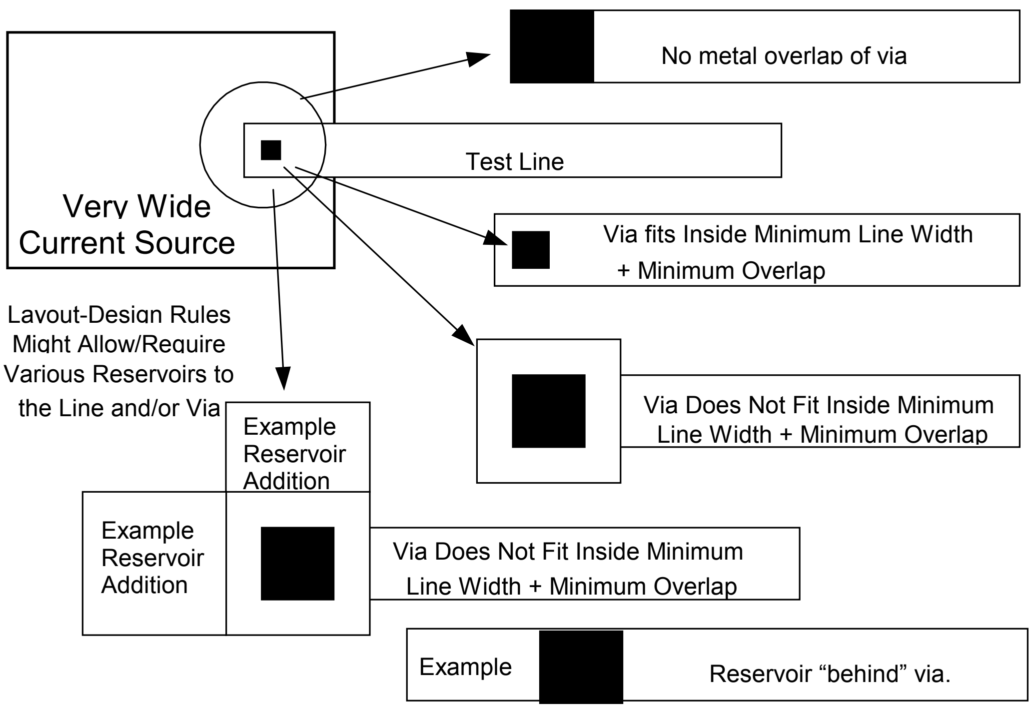

Figure 5 — Depending upon the individual design rules for minimum line width, via size, and metal overlap of via, line design will vary. However, it is important to use minimum design conditions to get an accurate understanding of EM for the metal system and design rules.

3 Electromigration test structure definition: Line and Via Structures (cont'd)

3.10 Document and report for each structure

- Metal level of test line
- Line Width
- Line Length
- If a test structure length other than the standard 400 µm is used, also include a description of experimentation and results for non-standard length structure.
- Electron current source metal level
- Name and number of Vias at current source (cathode) end.
- Space between extrusion and stress line
- Figure showing any added metal reservoir in the region of the cathode via, if different than minimum design requirements.

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4 Stress-Induced-Void (SIV) structures

4.1 Serpentine structures

Figures 6 and 7 show two basic types of serpentine long lines: Figure 6 without a bridging monitor (lines can be shorted internally) is not recommended (but not excluded), and **Figure 7 with a bridging monitor that is recommended**.

For each metal level to be evaluated:

- Kelvin Connection
- Three Structures: Width = 1) Wmin, 2) 1.3*Wmin, and 3) 2*Wmin - where Wmin is the minimum design line width.
- Total Length >= 5,000 µm (0.5 mm)
- Minimum space between lines

Document and Report the following for each structure:

- Line Width
- Total serpentine Length
- Space between lines

4.2 Via and line structures

Narrow via-line structures defined in section 3 can also be used to evaluate SIV where stress around vias interact with lines.

4 Stress-Induced-Void (SIV) structures (cont'd)

Figure 6 — Example Kelvin connected, serpentine SIV structure, *without bridging monitor* lines. This variation is *Not Recommended*.

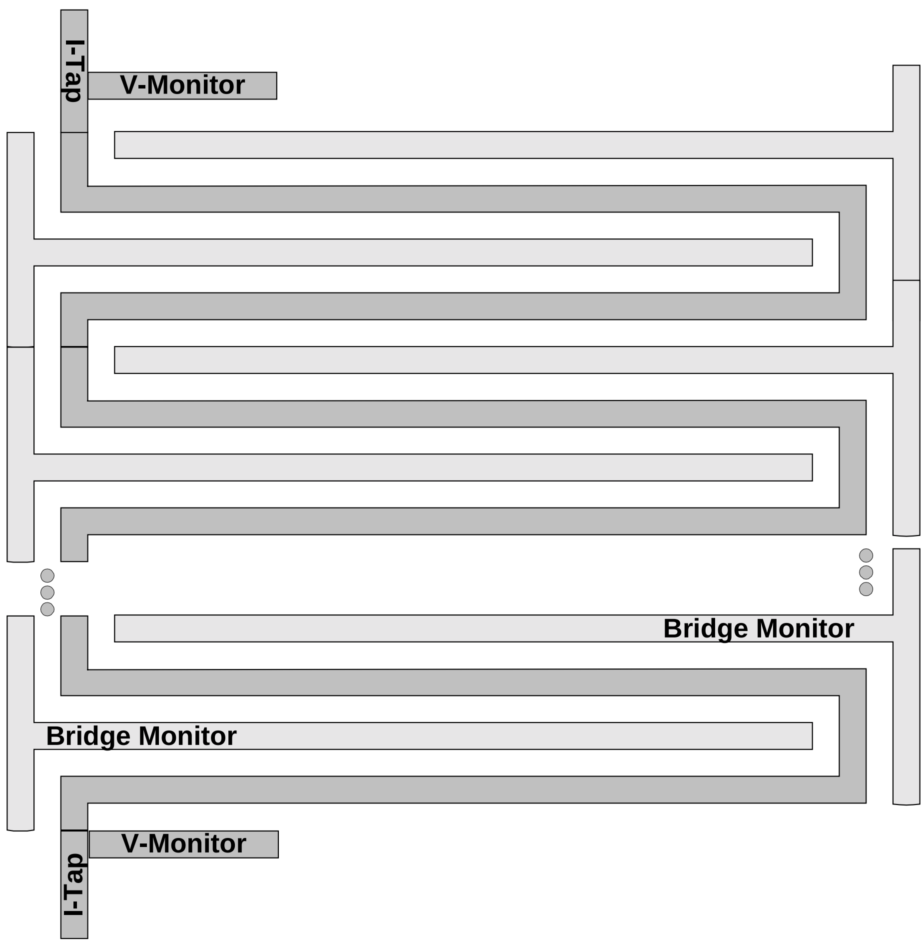

Figure 7 — Example Kelvin connected, serpentine SIV structure, *with bridging monitor* lines. This variation *Is Recommended*.

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